

AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

1 Claim 1. (currently amended) A state machine input/output circuit responsive
2 to a clock signal having cyclically repeating rising edges and falling edges, for
3 providing data to an output port, comprising:

4 a memory having a plurality of storage elements, each storage element
5 being adapted to store a bit and provide the bit as an output of said memory
6 ~~having an input and an output, said input being programmably connectable to~~
7 ~~either a state machine, microprocessor, or other programmably controllable data~~
8 ~~source for selection of data for storage therein;~~

9 a first multiplexer having a multiplexer ~~an~~ output, having a plurality of
10 inputs receiving the outputs of said memory, and having a control input for
11 selecting, in response to a control signal, an input for connection to said
12 multiplexer output;

13 a control signal generator connected to the control input of the first
14 multiplexer for generating a control signal to control said first multiplexer to select
15 said first multiplexer inputs for connection to said first multiplexer output; and

16 a clock edge selector circuit connected to said first multiplexer for
17 providing, in response to an edge select signal, the output of said first multiplexer
18 to said output port selectably on either said rising edges or said falling edges of
19 said clock signal.

1 Claim 2. (currently amended) The state machine input/output circuit of Claim
2 1, wherein said clock edge selector circuit, wherein ~~further comprises:~~

3 the inputs ~~input~~ of the first and second flip-flops are connected ~~coupled~~ to
4 the output of said multiplexer, said first flip-flop changing states on said rising

5 edge of clock pulse and said second flip-flop changing states on said falling edge
6 of clock pulse;

7 the outputs output of said first and second flip-flops are connected
8 ~~coupled~~ to first and second inputs of a second multiplexer;

9 the control input of said second multiplexer is connected ~~coupled~~ to the
10 output of an edge select register; and

11 the output of said second multiplexer is connected ~~coupled~~ to said output
12 port.

1 Claim 3. (original) The state machine input/output circuit of Claim 1, further
2 comprising a plurality of said input/output circuits, for providing data to a plurality
3 of output ports, wherein said output ports are connected on an output data bus.

Claim 4. (canceled)

1 Claim 5. (currently amended) A state machine input/output circuit responsive
2 to a clock signal having cyclically repeating rising edges and falling edges, for
3 passing data from an input port to a sampled output port, comprising:

4 a clock edge selector circuit having an input connected ~~coupled~~ to said
5 input port and having an output, for selecting, in response to an edge select
6 signal, data on said input port for provision to said selector circuit output
7 selectably on either said rising edges or said falling edges of said clock signal;

8 a first multiplexer having a multiplexer an output connected ~~coupled~~ to a
9 first flip/flop, said multiplexer having two inputs, a first one of said inputs
10 receiving said selector circuit output, and a second one of said inputs connected
11 ~~coupled~~ to the output of said first flip/flop and to the sampled output port, and

12 having a control input for selecting, in response to a control signal, said first input
13 or said second input for connection to said first multiplexer output;

14 a control signal generator connected to a second multiplexer for
15 generating a control signal to control said a second multiplexer to select said
16 second multiplexer inputs for connection to said second multiplexer output;

17 a memory having a plurality of storage elements, each storage element
18 being adapted to store a bit and provide the bit at a memory output of said
19 memory having an input and an output, said input being programmably
20 connectable to either a state machine, microprocessor, or other programmably
21 controllable data source for selection of data for storage therein, said memory
22 outputs being connected to the inputs of said second multiplexer, wherein the
23 output of said second multiplexer selects said first input or said second input of
24 said first multiplexer for connection to said first multiplexer output.

1 Claim 6. (currently amended) The state machine input/output circuit of Claim
2 5, wherein ~~said clock edge selector circuit further comprises:~~

3 an input to said clock edge selector circuit is connected ~~coupled~~ to the
4 input of a second and a third flip-flop being clocked at said state machine clock
5 rate, said second flip-flop changing states on said rising edge of clock and said
6 third flip-flop changing states on said falling edge of clock;

7 the outputs ~~output~~ of said second and third flip-flops are connected
8 ~~coupled~~ to first and second inputs of a third multiplexer;

9 the control input of said third multiplexer is connected ~~coupled~~ to the
10 output of a edge select register; and

11 the output of said third multiplexer is connected ~~coupled~~ to said output of
12 said clock edge selector circuit.

1 Claim 7. (currently amended) The state machine input/output circuit of Claim
2 5, further comprising a plurality of said input/output circuits, for passing data from
3 an input port to a sampled output port, wherein said input port is ~~inputs are~~
4 connected to ~~on~~ an input data bus and said sampled output port is ~~outputs are~~
5 connected to ~~on~~ an output bus.

Claim 8 (canceled)

1 Claim 9. (currently amended) A state machine input/output circuit responsive
2 to a clock signal having cyclically repeating rising edges and falling edges, for
3 passing output data to an output port, comprising:

4 a memory having a plurality of storage elements, each storage element
5 being capable of storing a bit and providing the bit as an output of said memory
6 ~~having an input and an output, said input being programmably connectable to~~
7 ~~either a state machine, microprocessor, or other programmably controllable data~~
8 ~~source for selection of data for storage therein;~~

9 a first multiplexer having an output, having a plurality of inputs receiving
10 the outputs of said memory, and having a control input for selecting, in response
11 to a control signal, an input for connection to said output;

12 a control signal generator connected to said first multiplexer for generating
13 a control signal to control said first multiplexer to select cyclically said first
14 multiplexer inputs for connection to said first multiplexer output;

15 a second multiplexer having a first input and a second input, having an
16 output, and having a control input for selecting, in response to a control signal,
17 an input for connection to said second multiplexer output, said first input being
18 connected ~~coupled~~ to a predetermined output data source, said output being
19 connected ~~coupled~~ to a data ~~the control~~ input of a first flip-flop being clocked at
20 said state machine clock rate, said second input being connected ~~coupled~~ to an

21 the output of said first flip-flop and to the input of a clock edge selector circuit,
22 and said control input being connected to said output of said first multiplexer;
23 said clock edge selector circuit connected to said second multiplexer for
24 providing, in response to an edge select signal, the output of said second
25 multiplexer to said output port selectably on either said rising edges or said
26 falling edges of said clock signal.

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